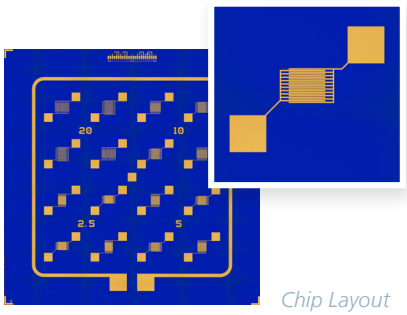
Fraunhofer IPMS

Substrates for Material Characterization

Organic semiconductors are key components in organic electronics and photovoltaics. They are used to create flexible electronic devices and solar cells that convert sunlight into electricity. Their unique properties offer advantages such as flexibility and environmentally friendly, low-cost manufacturing.
Typical for this class of materials are low temperature processes and large area deposition and structuring with various coating and printing processes. The active semiconductor materials determine the performance of the entire system considerably. That is why an easy-to-use and reliable electronic characterization of these semiconductors is an essential prerequisite for material and process developers.



Chip Layout

Fraunhofer IPMS offers standardized and customer-specific transistor structures in bottom-gate architecture. These substrates enable the characterization of conducting and semiconducting materials like organic semiconductors for thin-film gas sensors.

They are essential for material development and testing as well as for quality control. Optimum measurement results can be achieved by adapting the chips in terms of chip size, design and dielectric layer thickness.

The following properties are mostly of interest:

- Conductivity
- Charge carrier mobility
- Contact resistance
- On/Off current ratio

To simplify the measurement procedures of OFET substrates, Fraunhofer IPMS has also developed a hand prober. This OFET miniprober allows fast and easy measurements by reliable pad contacting.

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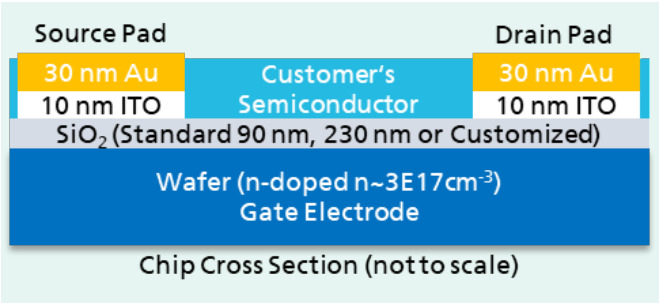
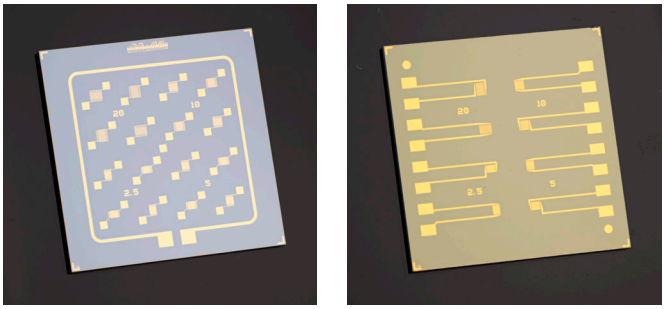


OFET Wafer Stack for Semiconductor Testing



Exemplary OFET Chip Layouts

Chips for Organic Field Effect Transistors (OFET)

If an organic semiconductor layer is deposited on such a substrate, the Si-bulk acts as gate electrode and controls the channel current between the gold electrodes on top. A suitably doped Si-SiO2 interface in CMOS quality guarantees a reproducible gate contact. Gold electrodes with a patented undercoating suppress the formation of injector barriers between the gold electrodes and the organics in the transistor channel. This guarantees reliable ohmic source / drain contacts in the OFET even for p-type semiconductors. Due to both reliability and reproducible preparation, these substrates are applied for standardized material screening by all key developers of organic semiconductors all over the world.

In the standard OFET layout, a 200 mm wafer has almost 1800 individual transistors on 112 chips, each sized at 15 × 15 mm². Each chip carries four groups with four identical transistors, with a channel length of 2.5, 5, 10, 20 µm respectively (see top left). Identical layouts with graded channel widths as well as a flexible selection of the oxide thickness allow the adjustment to a broad voltage and conductivity range of the test materials. Customer-specific layouts with different electrode geometries are possible at any time. In advantage for our customers, beside the wafers we offer waffle packs with 16 seperated chips.

Advantages

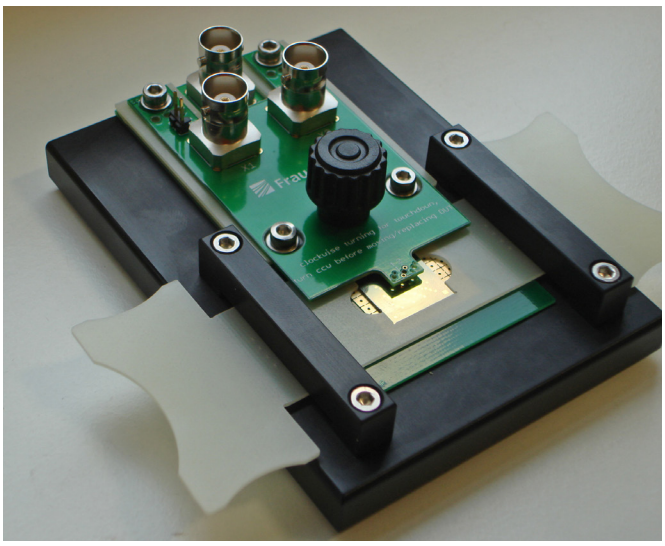
- Various designs and channel sizes on one chip
- Large channel lengths possible
- Different orientations of the transistors
- High reproducibility and precision
- Adjustable gate oxide thickness
- Low leakage current
- Top gate contact for easy contacting

OFET Miniprober

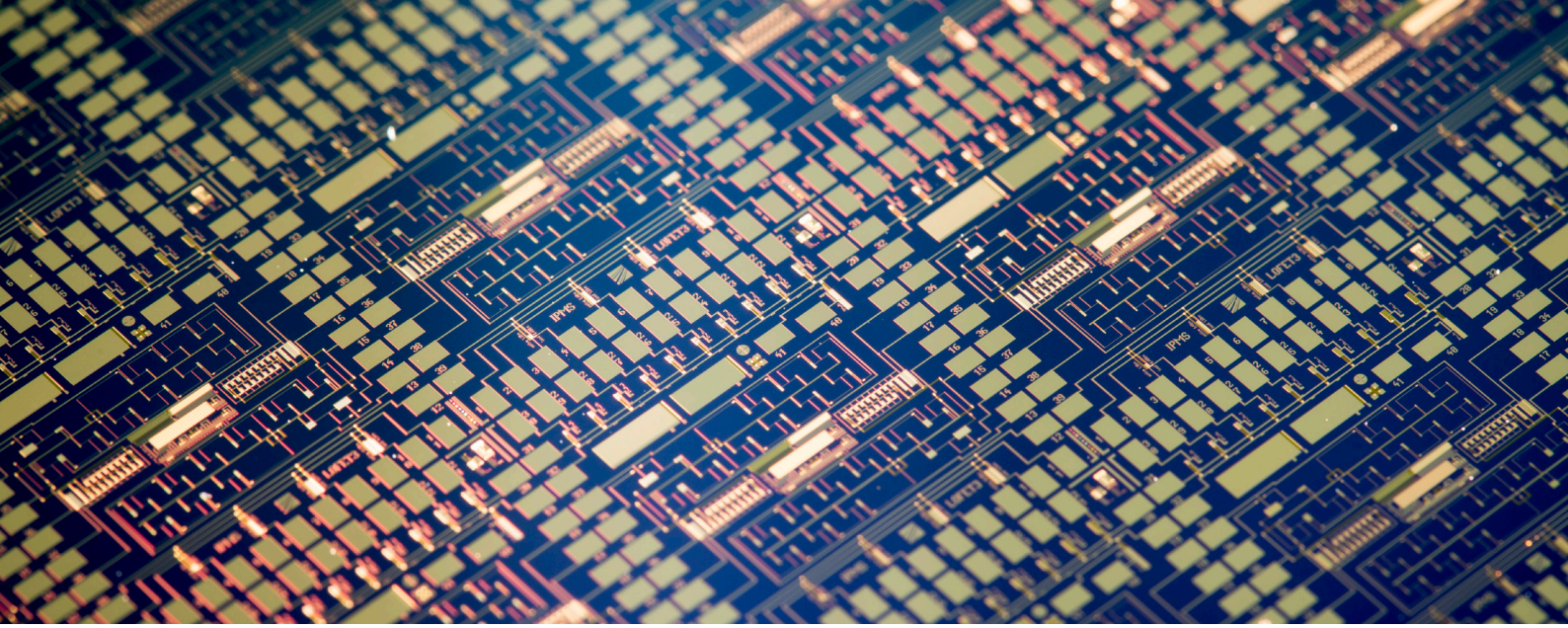
Easy to use and quick measurements without expensive prober stations. With a given substrate size, pad grid and pad arrangement in large batches, Fraunhofer IPMS has developed a miniprober (top right). It has two electric connections on the front (source and drain) and one connection on the back (gate) and does not require probe station, samplers or manipulator pins. A reliable interconnection is established on contact pads, which are only 0.5 × 0.5 mm² in size. Customized versions of the miniprober varying the connection arrangement, the position and number of the pads are possible. This makes the miniprober suitable for other applications in addition to OFETs. Signals are transmitted to the measurement instrument by BNC or triax cables.

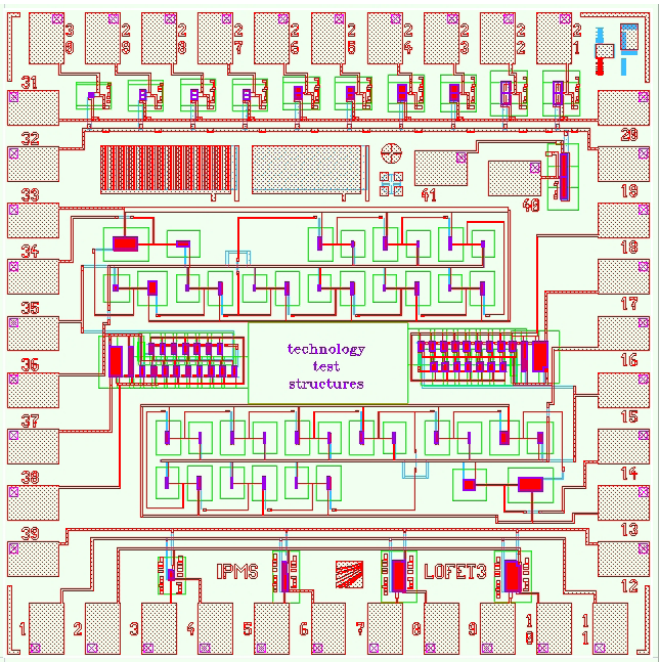
Advantages

- No probing system required
- Easy DUT handling
- Stable and secure connection
- Other chip sizes or pad arrangements possible



OFET Miniprober





Layout of the Basic Logic Circuit with LOFET

Basic Logic Circuits with Lateral Organic Field Effect Transistors (LOFET)

One further step in simplifying materials characterization is the analysis of basic logic circuits. Here, up to 36 single transistors are interconnected to inverters and ring oscillators. Monitoring of the active materials then only requires a frequency measurement of the ring oscillators which can be automated easily. This prevents the complicated and time-consuming measurement and analysis of the individual transistor characteristic. Furthermore, it is not only reliable information about logic capability that is acquired. The dynamic characteristics of the inverters are also determined.

The layout of a LOFET chip (Figure 1) includes an initial block with eleven individual transistors making a complete parameter extraction for circuit simulation possible. A second block contains four inverters which are replicated in the oscillators. These separately accessible inverter levels enable a detailed analysis of the transient behavior in case the amplification of the individual inverter stages is not sufficient for starting the oscillation of the ring oscillators. The third block contains ring oscillators with either 7 or 15 stages. Each ring circuit has a three-stage output amplifier which decouples the oscillation inside the ring from the output terminal and allows a direct frequency measurement without external amplification. The LOFET substrates are also produced in bottom gate architecture so that functional circuits require the deposition of the semiconductor layer only.

Product Portfolio

characteristics	bare OFET	OFET Gen4, 90 nm SiO_2	OFET Gen4, 230 nm SiO_2	OFET Gen5	OFET AX1579	OFET AX1580	OFET AX1581	Customized OFET	LOFET
Wafer Substrate 150 mm or 200 mm	●	●	●	●	●	●	●	●	●
gate: n-doped silicon (doping at wafer surface: n~3e17 cm-3)	●	●	●	●	●	●	●	●	○
SiO_2 90 nm	○	●	○	○	○	○	○	○	○
SiO_2 200 nm	○	○	○	○	○	○	○	○	●
SiO_2 230 nm	●	○	●	●	●	●	●	○	○
SiO_2 thicknesses between 10 nm and 500 nm	◑[1]	◑[1]	◑[1]	◑[1]	◑[1]	◑[1]	◑[1]	◑[1]	○
drain/source: 30 nm Au with 10 nm ITO	○	●	●	●	●	●	●	●	○
Design Gen 4:									
4 x transistors L=2.5 µm, W=10 mm	○	●	●	○	○	●	●	○	○
4 x transistors L=5 µm, W=10 mm									
4 x transistors L=10 µm, W=10 mm									
4 x transistors L=20 µm, W=10 mm									
Design Gen 5:									
4 x transistors L=2.5 µm, W=2 mm	○	○	○	●	○	○	○	○	○
4 x transistors L=5 µm, W=2 mm									
4 x transistors L=10 µm, W=2 mm									
4 x transistors L=20 µm, W=2 mm									
Design AX1579:									
4 x transistors L=10 µm, W=2 mm	○	○	○	○	●	○	○	○	○
4 x transistors L=20 µm, W=2 mm									
4 x transistors L=40 µm, W=2 mm									
4 x transistors L=80 µm, W=2 mm									
Easy access to bondpads	○	○	○	○	○	●	○	◑[3]	○
Heater	○	○	○	○	○	○	●	◑[3]	○
Source/drain layer: Ti/ TiN, Rs about 10 Ω/sq. with 30nm Au with 10 nm ITO top layer	○	○	○	○	○	○	○	○	●
Design:	○	○	○	○	○	○	○	○	●
transistors, inverters and ring oscillators									
Customized design								●	
Compatibility OFET prober	○	●	●	●	●	○	◑[2]	◑[3]	○
Package: waffle pack (16 chips)	◑[1]	● Part 2028	● Part 1897	◑[1]	● Part 2035	● Part 2036	● Part 2037	●	◑[1]
Package: diced on foil (60 chips)	● Part 176	○	○	● Part 175	● Part 2472	● Part 2030	● Part 2031	◑[3]	◑[1] Part 267
Package: diced on foil (112 chips)	◑[1]	● Part 2017	● Part 1301	○	○	○	○	◑[3]	○

○ Feature non-existent
● Feature available
◑ Feature partly available (see restrictions)

[1] Available on request
[2] Measurement works with OFET prober
[3] Depending on customer design